IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent: 6,475,846

Date of Issue: November 5, 2002

Name of Patentee: Marotta et al.

Title of Invention: METHOD OF MAKING FLOATING-GATE MEMORY-CELL ARRAY WITH DIGITAL LOGIC TRANSISTORS

PROPOSED DRAWING AMENDMENT UNDER 37 CFR §1.173(b)(3)

October 22, 2003

Box REISSUE
Assistant Commissioner for Patents
Washington, D.C. 20231

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
I hereby certify that the above correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231 on October 22, 2003.

Robert N. Rountree, Reg. No. 39,347

Dear Sir:

Please change the Vdd label of Figure 1 at the source of transistor 27 to Ground in agreement with the Ground symbol as marked in red on the attached figure. Two paragraphs from column 4 of the specification are amended to agree with the drawing amendment. No new matter is added.

Respectfully submitted,

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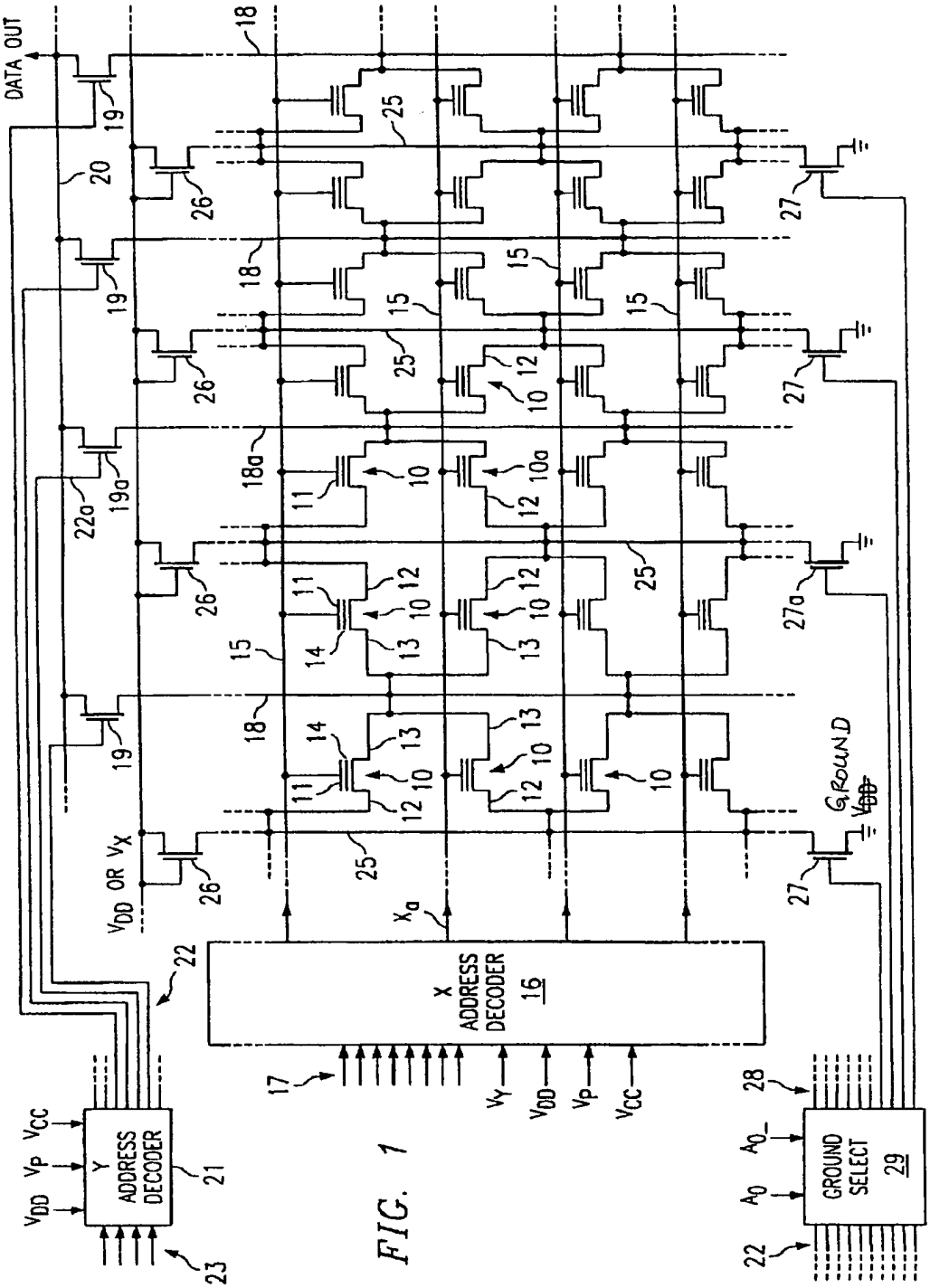
DATA OUT
18
19
20
26
25
27
15
12
10
18a
19a
22a
10a
11
27a
13
14
V_{DD} OR V_X
X_a
22
X ADDRESS DECODER 16
17
V_Y
V_{DD}
V_P
V_{CC}
28
A_0
$\overline{A_0}$
GROUND SELECT 29
Y ADDRESS DECODER 21
23
GROUND
V_{SS}

FIG. 1